Please amend claim 15 as follows.

IN THE CLAIMS (Entire set)

1. (Original) A system comprising:

first, second, third and fourth modules;

a circuit board including first, second, third, and fourth module connectors to receive the first and second modules, respectively;

a first group of paths of conductors extending from the circuit board to the first module connector, to the first module, back to the first module connector, to the circuit board, to the second module connector, to the second module, back to the second module connector, to terminations, wherein the first group of paths include a first short loop through section in the first module and a second short loop through section in the second module, to each couple to stubs for corresponding first and second chips of the first and second modules; and

a second group of paths of conductors extending from the circuit board to the third module connector, to the third module, back to the third module connector, to the circuit board, to the fourth module connector, to the fourth module, back to the fourth module connector, to terminations, wherein the second group of paths include a first short loop through section in the third module and a second short loop through section in the fourth module, to each couple to stubs for corresponding first and second chips of the third and fourth modules.

2. (Original) The system of claim 1, wherein the terminations of the first and second paths are on the circuit board.

3. (Original) The system of claim 1, further comprising a buffer on the first, second, third, and fourth modules.

4. (Original) The system of claim 1, further comprising error correction code chips on the first, second, third, and fourth modules.

5. (Original) The system of claim 1, further comprising a fifth module coupled through the first group of paths between the first and second modules.

6. (Original) The system of claim 1, further comprising a sixth module coupled through the second group of paths between the third and fourth modules.

7. (Original) The system of claim 1, wherein chips on the first, second, third, and fourth modules are designed to receive four data lines.

8. (Original) The system of claim 1, wherein the circuit board is a printed circuit board and a motherboard.

9. (Original) A system comprising:

first, second, third and fourth modules;

a circuit board including first, second, third, and fourth module connectors to receive the first and second modules, respectively;

a first group of paths of conductors extending from the circuit board to the first module connector, to the first module, back to the first module connector, to the circuit board, to the second module connector, to the second module, back to the second module connector, to terminations of the circuit board, wherein a first section of each of the first group of paths couples to stubs for corresponding first, second, third and fourth chips of the first module, and a second section of each of the first group of paths couples to stubs for corresponding first, second, third, and fourth chips of the second module; and

a second group of paths of conductors extending from the circuit board to the third module connector, to the third module, back to the third module connector, to the circuit board, to the fourth module connector, to the third module, back to the fourth module connector, to terminations of the circuit board, wherein a first section of each of the second group of paths couples to stubs for corresponding first, second, third, and fourth chips of the third module, and a second section of each of the first group of paths couples to stubs for corresponding first, second, third, and fourth chips of the fourth module.

10. (Original) The system of claim 9, wherein chips on the first, second, third, and fourth modules are designed to receive eight data lines.

11. (Original) The system of claim 9, further comprising a buffer on the first, second, third, and fourth modules.

12. (Original) The system of claim 9, further comprising error correction code chips on the first, second, third, and fourth modules.

13. (Original) The system of claim 9, further comprising a fifth module coupled through the first group of paths between the first and second modules.

14. (Original) The system of claim 9, further comprising a sixth module coupled through the second group of paths between the third and fourth modules.

15. (Currently amended) A system comprising:

first, second, third and fourth modules;

a circuit board including first, second, third, and fourth module connectors to receive the first and second modules, respectively;

a first group of paths of conductors extending from the circuit board to the first module connector, to the first module, back to the first module connector, to the circuit board, to the second module connector, to the second module, back to the second module connector, to terminations of the circuit board;

a second group of paths of conductors extending from the circuit board to the third module connector, to the third module, back to the third module connector, to the circuit board, to the fourth module connector, to the third module, back to the fourth module connector, to terminations of the circuit board; and

wherein the first, second, third, and fourth module connectors are such that chips on the first, second, third, and fourth modules ~~may be chips with~~ are chips designed to receive either N or N/2 data lines, wherein the first and second group of paths provide the data lines.

16. (Original) The system of claim 15, wherein if the chips are designed to receive N/2 data lines:

a first section of each of the first group of paths, which are short loop through sections, couples to stubs for corresponding first and second chips of the first module, and a second section of each of the first group of paths, which are short loop through sections, couples to stubs for corresponding first and second chips of the second module; and

a first section of each of the second group of paths, which are short loop through sections, couples to stubs for corresponding first and second chips of the third module, and a second section of each of the first group of paths, which are short loop through sections, couples to stubs for corresponding first and second chips of the fourth module.

17. (Original) The system of claim 15, wherein if the chips are designed to receive N data lines:

a first section of each of the first group of paths couples to stubs for corresponding first, second, third and fourth chips of the first module, and a second section of each of the first group of paths couples to stubs for corresponding first, second, third, and fourth chips of the second

module; and

a first section of each of the second group of paths couples to stubs for corresponding first, second, third, and fourth chips of the third module, and a second section of each of the first group of paths couples to stubs for corresponding first, second, third, and fourth chips of the fourth module.

18. (Original) The system of claim 15, wherein N is eight.

19. (Original) The system of claim 15, further comprising a buffer on the first, second, third, and fourth modules.

20. (Original) The system of claim 15, further comprising error correction code chips on the first, second, third, and fourth modules.

21. (Original) The system of claim 15, further comprising a fifth module coupled through the first group of paths between the first and second modules.

22. (Original) The system of claim 15, further comprising a sixth module coupled through the second group of paths between the third and fourth modules.